# A Novel ECT System Based on FPGA and DSP

Xuehui Zhang[1,2], Huaxiang Wang[1], Ziqiang Cui[1] and Lei Tang[1]
*1. School of Electrical Engineering and Automation, Tianjin University, Tianjin, 300072 China*
*2. School of Electrical Engineering and Automation, Hebei University of Technology, Tianjin, 300130 China*
*zhangxuehui@hebut.edu.cn*

## Abstract

*Previous analogue designs have many associated problems such as noise, component mis-matching, input offset and so on, and their speed is limited by some factors such as switching transients, multiplexing overhead and conversion delays. To improve the precision and speed of the system, a novel 16-electrode digitized electrical capacitance tomography system based on field programmable gate array (FPGA) and digital signal processor (DSP) is designed. FPGA performs the system logical control, produces sine wave exciting signal and realizes digital demodulation, which greatly simplifies the control and interface circuit and improves the reliability of the system. While DSP accomplishes image reconstruction, then sends grey levels to host computer through PCI bus to display the cross section image. The results of theoretic analysis and experiment show that both systematic SNR and speed are improved effectively.*

## 1. Introduction

Electrical capacitance tomography (ECT) techniques have been developed to visualize industrial processes with dielectric materials. ECT is based on measuring capacitances from a sensor with multiple electrodes and reconstructing cross sectional or tomographic images of permittivity distribution from the measurement data.

The speed and the precision are two important performance indexes of the ECT system. Special integrated direct digital synthesis (DDS) chips (e.g. AD7008) are normally used in analogue ECT system to produce sine exciting signal, but its signal noise radio(SNR),control mode and frequency setting speed are restricted. The analogue filter and the demodulator have been a bottleneck of imaging precision and speed since it is difficult to shorten settling time of the low pass filter while maintaining high accuracy. Besides, image reconstruction algorithm is usually performed by host computer, which can be speeded up by digital signal processor (DSP) which is powerful on digital processing [1].

To overcome the shortcomings of the existing analogue system, a novel 16-electrode digitized electrical capacitance tomography system based on FPGA and DSP is designed. The majority of the system is implemented by using firmware-upgradeable digital components, which will make it easy for debugging and future upgradeability.

## 2. Architecture of the system

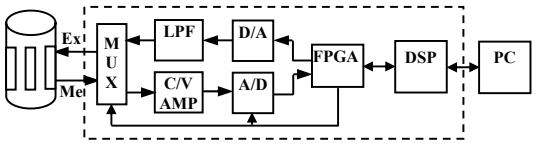


**Figure 1. Digital ECT system architecture**

The digitized ECT system has three main units as shown in Figure 1: (1) the sensor, (2) the data acquisition and processing unit and (3) the computer. The sensor consists of a set of electrodes symmetrically mounted outside or inside an insulating pipe. The data acquisition and processing unit is mainly consisted of FPGA and DSP, it measures the capacitances for all possible electrode combinations under the control of FPGA and sends data to DSP which takes charge of the image reconstruction algorithm and communication with the host computer. The host computer in this system is mainly used to provide a GUI and display the tomographic images.

## 3. FPGA and DSP

DSP has two buses and two separate memories, which makes it ideally fit for performing numerically

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intensive mathematical operations at relatively high speeds. Whereas it will be a very challenging design task to utilize DSP to control a considerable number of external devices (e.g. 32 or more ADCs) because of the very limited number of direct physical connections. While FPGA is ideally suitable for multi-tasking since it offers significant benefits including improved computational capabilities and higher bandwidths than most DSPs. FPGA may be used to speed data acquisition, relieving DSP from the impractical burden of handling external devices and pre-processed acquired data.

The digitized ECT system makes full use of advantages of FPGA and DSP. FPGA takes charge of fast data-acquiring and pre-processing, whereas DSP performs the image reconstruction algorithm and communicates with PC via PCI bus. Texas Instrument 32-bit fixed point digital signal processor TMS320C6416 DSP and Xilinx XC2VP30 FPGA of Virtex II Pro series are chosen for this system.

## 4. DDS based on FPGA

Since the ECT inverse problem is severely ill-posed [2] and the measured voltage signal produced by capacitance changes in ECT pipe is very weak, it requires that the applied and measured signals have very high precision. Presently, most PT research groups use integrated DDS chips as sine wave generator, such as AD7008. Although it possesses of much functions, its control mode and frequency setting rate can't satisfy perfectly the real time requirement.

FPGA offers design flexibility and scalability. Frequency, phase and amplitude of the signal generator based on FPGA can be easily controlled. Moreover, it can produce arbitrary wave including multi-frequency signal without modifying peripheral hardware. Besides, logic control of the system is integrated in the FPGA, which will greatly simplify the interface circuit and improve the stability of the whole system.

### 4.1. Principle of DDS

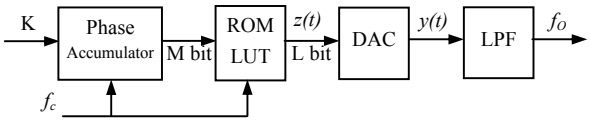



**Figure 2. Configuration of DDS**

A direct digital synthesizer (DDS) is a numerically controlled oscillator employing a phase accumulator, sine and cosine look-up tables, a D/A converter (DAC) and a low pass filter (LPF). Figure 2 shows the essential configuration of a DDS [3].

The output frequency $f_o$ is

$$f_O = K \cdot f_c / 2^N \qquad (1)$$

Where $f_c$ is the system clock frequency, $K$ is the frequency control word, and $N$ is the number of bits of phase accumulator, $K<2N$-1.Therefore the frequency resolution of the DDS is $\triangle f = f_c/2^N$. Signal at any frequency can be obtained by setting $N$, $K$ and $f_c$.

### 4.2. FPGA design

Phase accumulator is a key part in designing. Although the adder in FPGA library can realize 32-bit phase accumulator easily, a relative large delay will occur when operation frequency is high. Four 8-bit accumulators are used to accomplish a 32-bit accumulator in pipeline mode. The result simulated by the software development tool ise8.1 supplied by Xilinx shows that pipeline technology enhances the systematic speed obviously.

The scale of the ROM in DDS increases exponentially according to data width, while resources consuming is a main problem in designing the phase-to-amplitude conversion circuit. In order to save resources, only a quarter of quantified amplitudes is stored in the ROM table. The full period of quantified amplitudes is obtained through appropriate address transform, three quarters resources are saved.

HDL (Hardware Description Language) is used in the FPGA design, IP Core (Intellectual Property Core) in ise8.1 is fully utilized to configure DDS module. Both reliability and real time performance are improved.

### 4.3. Output of the DDS

The digital output of FPGA needs to be converted into analogue sine wave by DAC. The system adopts a 14-bit, 125 MSPS, low power CMOS DAC, AD9754.

AD9754 has high Spurious Free Dynamic Range (SNFR), it is of 83dB when the output frequency is 5MHz. Whereas the DAC in AD7008 is of 10-bit and its SNFR is of 50dB only. Both precision and SNR of the signal source are obviously improved compared with AD7008. The highest harmonic frequency appears at $(f_c/f_o\text{-}1)f_o$, the systematic SNR will be enhanced further by adding a low pass filter behind.

As a result, combined with AD9754, XC2VP30 FPGA realizes the DDS. The parameters are following as: system clock frequency $f_c$, phase accumulator width $N$ and frequency resolution $\triangle f$ equals 50MHz, 32 and 0.0117Hz, respectively; the range of output frequency $f_o$ is 0 to 25 MHz. Two orthogonal sine waves at 500 KHz are produced for the ECT system. Figure 3 shows

the output wave simulated in ModelSim 6.0 supplied by Xilinx. The wave is smoother than that of AD7008 since the precision of DAC enhances 4 bits.

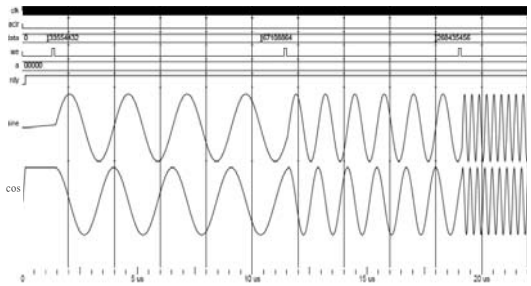



**Figure 3. Output of the DDS**

## 5. PSD (phase sensitive demodulation)

Previous ECT system widely adopts analogue filter and demodulation, which limit the speed and precision of tomography due to the performance of the analogue devices. Besides, two DDS chips are used in the previous ECT system, one produces exciting signal, another provides reference signal for demodulation. Although the two DDS chips are based on a same crystal oscillator, they can hardly generate rigidly synchronized signals in frequency and phase, which will influence the result of demodulation.

Digital demodulation overcomes the shortcomings. Reference signals for demodulation are generated by FPGA as it produces the sine wave exciting signal, which assures the accuracy of the demodulation. At the same time, the scheme of integrating DDS module and PSD module in one FPGA chip enhances the systematic SNR and simplifies the peripheral circuit.

Quadrature demodulation is adopted in the design. Figure 4 shows the framework of digital quadrature demodulation.

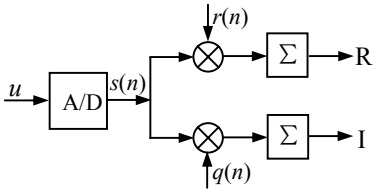



**Figure 4. Digital quadrature demodulation**

Assume that there are $N$ sample points in every ADC cycle, $s(n)$ is the sampled signal, $r(n)$ and $q(n)$ are in phase and quadrature phase signals respectively, where $0 \leqslant n \leqslant N\text{-}1$. When the $N$ is even, according to the orthogonality of triangle function, the following formulae can be derived,

$$R = \sum_{n=0}^{N-1} r(n)s(n) = \sum_{n=0}^{N-1} \cos(\frac{2\pi}{N}n) A\cos(\frac{2\pi}{N}n + \theta)$$

$$= NA\frac{1}{2}\cos\theta \qquad (2)$$

$$I = \sum_{n=0}^{N-1} q(n)s(n) = \sum_{n=0}^{N-1} \sin(\frac{2\pi}{N}n) A\cos(\frac{2\pi}{N}n + \theta)$$

$$= NA\frac{1}{2}\sin\theta \qquad (3)$$

The amplitude $A$ of $s(n)$ which stands for the measured voltage or capacitance can be obtained directly inside the FPGA utilizing the cordic IP core which can translate rectangular coordinates to polar coordinates based on the equation $A = \sqrt{R^2 + I^2}$. Alternatively, it can also be accomplished in DSP by calling the 'sqrt' function from dsplib provided by TI.

## 6. Image reconstruction

Image reconstruction for ECT is to determine the permittivity distribution and hence material distribution over the cross section from capacitance measurements. Nowadays, the main image reconstruction algorithms for ECT include linear back projection (LBP), Landweber iteration, Newton Raphson, conjugate gradient method and Tikhonov regularization, etc.[2, 4]. LBP and Landweber iteration algorithm are used in the system.

### 6.1. Characteristic of reconstruction algorithm

Although mathematically not accurate, the LBP algorithm is still widely used for on-line image reconstruction because of its simplicity and convergence. The inverse sensitivity matrix $S^{-1}$ is replaced by $S^T$, giving an approximated solution,

$$g = S^T\lambda \qquad (4)$$

Where g is the $m\times1$ vector of normalized pixel grey levels, $m$ is the number of pixels divided on the basis of finite element method (FEM), λ is the $n\times1$ vector of normalized measured capacitance, $n$ is the number of independent capacitance measurement which is equal to $N(N\text{-}1)/2$, where $N$ is the number of electrodes.

In the digital ECT system, there are 16 electrodes, ($N$=16), then the independent measurements $n$ equals 120, the pixel number $m$ equals 480. Therefore, to obtain the 480×1 vector g is just to multiply a 480×120 matrix $S^T$ with a 120×1 vector λ.

Landweber iteration is a transformation of the steepest descent method, which is widely used in

optimization theory. It chooses the negative gradient of $f(\mathrm{g})$ as new search direction for the next iteration.

$$\mathrm{g}_{k+1} = \mathrm{g}_{\mathrm{k}} - \alpha_k \nabla f(\mathrm{g}_k) = \mathrm{g}_k - \alpha_k S^T (S\mathrm{g}_{\mathrm{k}} - \lambda) \quad (5)$$

Where $\alpha_{\mathrm{k}}$ is a positive scalar, which decides the $k$th step size.

As LBP algorithm, Landweber iteration algorithm is also realized mainly by matrix multiplication.

### 6.2. Real time performance

The speed of image reconstruction is a crucial problem in ECT system. It will take a long time to realize reconstruction algorithm by using a computer. Taking the fastest LBP algorithm for example, in a 16-electrode ECT system, the cross section is divided into 480 regions, it will take 14ms for a computer, which is configured with P4, 2.0GHz, 256M memory, to complete an image reconstruction, i.e. 70 frames per second [4]. For more complicated algorithm, it will take longer time. DSP has hardware multipliers, which are suitable for special operation such as digital filter, convolution and FFT. Its particular multiply-accumulate (MAC) instruction makes it fit for matrix operation. As mentioned above, matrix operation is the main operation in image reconstruction. Therefore DSP is ideal for image reconstruction.

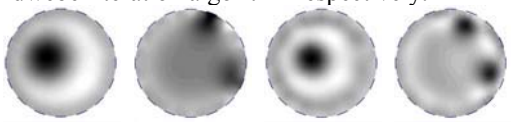
D F Garcia-Nocetti made use of TMS3206701 (133MHz) for LBP algorithm in a 12-electrode ECT system, the speed reached 135 frames per second [5]. Wang Mi made use of TMS3206202（250MHz）in a 16-electrode two-plane EIT system for LBP algorithm, it could capture 1000 frames/s per plane [6].

TMS3206416 (600MHz) [7] is chosen in the system. It has two hardware multipliers, four 16×16bit multiplications can be completed per cycle for total of 2400 million MACs per second. 57600 MACs need to be operated for accomplishing LBP algorithm given in equation (4). It will take 3.6ms for a computer, while only 24us will be taken using TMS3206416.

The time for reconstructing a frame of image is $t$, $t= n\times(t_1+t_2)+t_3+t_4$. Where $t_1$ is for data acquiring; $t_2$ is for A/D conversion; $t_3$ is for image reconstruction and $t_4$ is for PCI transmitting from DSP to PC, respectively. It is required 200ns for data acquiring, 0.1us for converting a data by AD9240 running at 10MHz; 24us for reconstructing a piece of image; 15us for transferring 480 grey values through the 32bit/33MHz PCI bridge of TMS3206416 from DSP to PC. Therefore, the time for reconstructing one image is $t$=120×(200×$10^{-3}$+0.1)+24+30=90us. The real time performance of image reconstruction is improved greatly.

### 6.3. Image results

Static experiments were carried out using the digitized ECT system. The vessel is a perspex pipe of 100mm in diameter, one or two perspex rods of 10mm in diameter were put in it. Figure 5 (a) - (d) show the image reconstruction results using LBP and Landweber iteration algorithm respectively.



**(a) LBP (b) LBP (c) Land. (d) Land.**

**Figure 5. Image results**

## 7. Conclusions

Actually, ECT is a real time signal processing system, the quantity of data is very big in its front end, which is featured with high speed and comparatively simple in operation architecture, FPGA is suitable for the pre-processing; whereas the quantity of data for post-processing is comparatively small, but its algorithm architecture is complicated, so it is necessary to use DSP featured with powerful signal processing ability to accomplish it.

In this paper, FPGA and DSP are fully utilized to construct a novel 16-electrode digitized ECT system. The systematic SNR and real time performance are both improved obviously.

## References


[1] W Q Yang, T A York, “New AC-based capacitance tomography system”, *Sci. Meas. Technol*, Vol.146, No.1, pp. 41-47, 1999.

[2] W Q Yang, Lihui Peng, “Image reconstruction algorithms for electrical capacitance tomography”, *Meas.Sci.Technol*, Vol.14, pp. R1-R13, 2003.

[3] Tierey J, Radar C, Gold B, “A digital frequency synthesizer”, *IEEE Trans Audio and Eletroacoust*, Vol.19, No.1, pp. 48-57, 1971.

[4] Lei Tang, “Research on Image Reconstruction Algorithms and Design of Software for EIT System”, M. Phil. dissertation, School of Electrical Engineering and Automation, Tianjin University, 2006.

[5] D F Garcia-Nocetti , J C Gamio, “Parallel Realization of the Linear Back-projection Algorithm for Capacitance Tomography Using TMS320C6701 Digital Signal Processors”, *3rd World Congress on Industrial Process Tomography*, Banff, Canada, Sep. 2003.

[6] Y Ma, N Holliday, Y Dai, M Wang, “A High Performance Online Data Processing EIT System”, *3rd World Congress on Industrial Process Tomography*, Banff, Canada, Sep. 2003.

[7] Texas Instruments, *TMS320C6416 fixed-point digital signal processors*, 2005.